Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	43	(conducting adj polymer) same (photosensitive)	US-PGPUB; USPAT	OR	ON	2005/07/13 08:18
L2	31	1 and @ad<"20010919"	US-PGPUB; USPAT	OR	ON	2005/07/13 08:46
L3	12	(conducting adj polymer) same (lithographical$2)	US-PGPUB; USPAT	OR	ON	2005/07/13 08:47
L4	7	3 and @ad<"20010919"	US-PGPUB; USPAT	OR	ON	2005/07/13 08:17
L5	0	(conducting adj polymer) same (lithographical$2)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/13 08:18
L6	11	(conducting adj polymer) same (photosensitive)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/13 08:18
L7	482	(three adj dimensional) and (conducting adj polymer) and @ad<"20010919"	US-PGPUB; USPAT	OR	ON	2005/07/13 08:46
L8	46	7 and (lithographical$2)	US-PGPUB; USPAT	OR	ON	2005/07/13 09:09
L9	287	(resist or photoresist) and (sidewall with (ripple or ribbed or rough))	US-PGPUB; USPAT	OR	ON	2005/07/13 09:44
L10	270	9 and @ad<"20040106"	US-PGPUB; USPAT	OR	ON	2005/07/13 09:43
L11	223	10 and (opening or recess or hole or trench or via)	US-PGPUB; USPAT	OR	ON	2005/07/13 09:44
L12	20	(resist or photoresist) and (sidewall with (ripple or ribbed or rough))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/13 09:30
L13	2479	438/221,296,426,431,424,435.ccls.	US-PGPUB; USPAT	OR	ON	2005/07/13 09:43
L14	2339	13 and @ad<"20040106"	US-PGPUB; USPAT	OR	ON	2005/07/13 09:46
L15	1600	14 and (resist or photoresist)	US-PGPUB; USPAT	OR	ON	2005/07/13 09:44
L16	1566	15 and (opening or recess or hole or trench or via)	US-PGPUB; USPAT	OR	ON	2005/07/13 09:45
L17	135	(substrate and (photoresist or resist) and sidewalls and liner).clm.	US-PGPUB; USPAT	OR	ON	2005/07/13 09:47
L18	118	17 and @ad<"20040106"	US-PGPUB; USPAT	OR	ON	2005/07/13 09:46

L19	0	(substrate and (photoresist or resist) and sidewalls and liner and (ribbed or ripple)).clm.	US-PGPUB; USPAT	OR	ON	2005/07/13 09:47

US-PAT-NO: 6537896

DOCUMENT-IDENTIFIER: US 6537896 B1

TITLE: Process for treating porous low k dielectric material in damascene structure to form a non-porous dielectric diffusion barrier on etched via and trench surfaces in the porous low k dielectric material

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Brief Summary Text - BSTX (19):

In the above referenced Kim U.S. patent application Ser. No. 09/932,527 the problem of **rough** edges from the rupturing of pores in porous low k dielectric material during the etching of openings for vias and/or trenches was solved by isotropic etching of the **rough sidewalls of the openings** to remove at least the peaks of the opened pores.

Brief Summary Text - BSTX (20):

The above referenced Kim and Chun U.S. patent application Ser. No. 10/032,666 solved the same problem of **rough** edges from the rupturing of pores in porous low k dielectric material by depositing a further layer of dielectric material over the **rough** edges of the opened pores of the etched **sidewalls of the openings** in the porous low k dielectric material.

US-PAT-NO: 6069091

DOCUMENT-IDENTIFIER: US 6069091 A

TITLE: In-situ sequential silicon containing hard mask layer/silicon layer plasma etch method

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Brief Summary Text - BSTX (8):

In addition, it is also recognized in the art of integrated circuit microelectronics fabrication that **sidewall** profiles of trenches formed within semiconductor substrates through conventional methods which employ a first plasma etch method in forming a composite patterned silicon nitride layer/patterned silicon oxide layer etch mask layer upon a semiconductor substrate and an independent second plasma etch method in forming a trench within the semiconductor substrate while employing the composite patterned silicon nitride layer/patterned silicon oxide layer as an etch mask layer are often **rough**.

Brief Summary Text - BSTX (9):

Inefficient use of integrated circuit microelectronics fabrication tooling and materials is undesirable within advanced integrated circuit microelectronics fabrication since integrated circuit microelectronics fabrication costs are thus increased. Similarly, **rough sidewall** profiles of shallow trenches formed within semiconductor substrates within integrated circuit microelectronics fabrications are also undesirable since such **rough sidewall** profiles may impede formation of isolation regions with optimal isolation characteristics within those shallow trenches and thus influence operating parameters of integrated circuit devices formed within adjoining active regions of a semiconductor substrate separated by the shallow trenches.